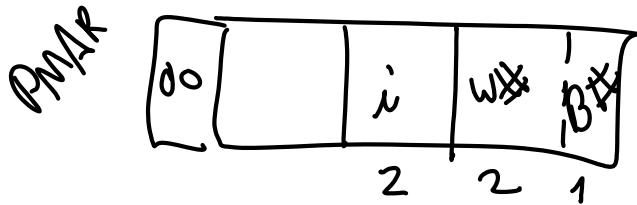


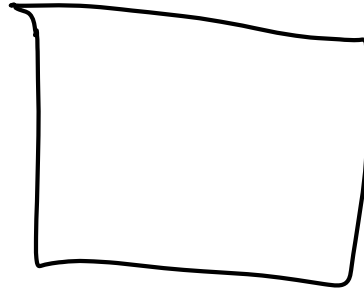
$$2^5 = 32B$$



16-bit Addr,
Byte' addrbl

words \rightarrow 2B

8B blocks \rightarrow $\frac{2B}{W}$ $\frac{4W}{BL}$



Mem 14-bit A

$$\rightarrow 2^{14} B = 16kB$$

VMEM 16-bit A

$$\rightarrow 2^{14} = 64kB$$

2-way SA

4 entries \rightarrow i 2bits

$$2^{14} B \left(\frac{W}{2B} \right) = 2^{13} W = 8kW$$

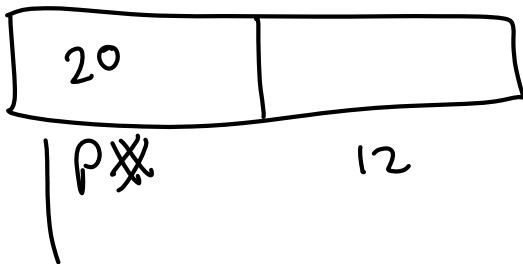
$$2^{14} B \left(\frac{W}{2B} \right) = 2^{15} = 32kW$$

$$2^{14} \left(\frac{6L}{8B} \right) = 2^{11} = 2kBL$$

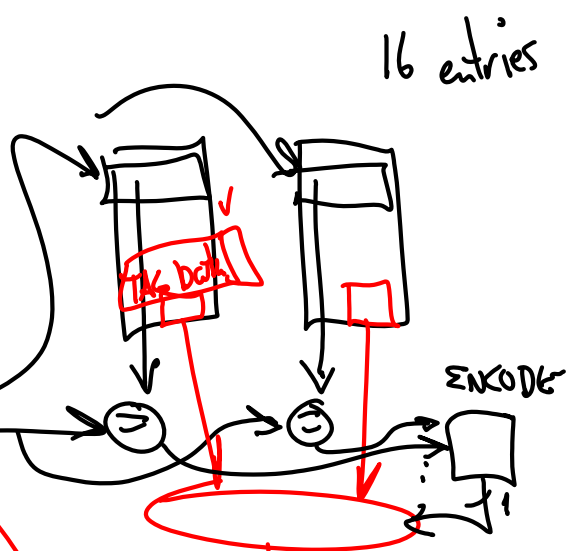
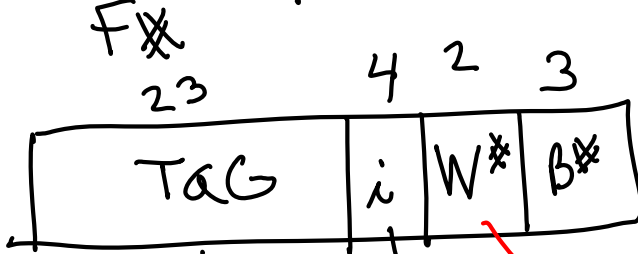
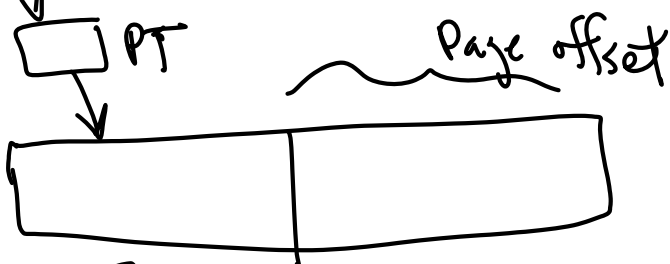
$$2^{14} \left(\frac{6L}{8B} \right) = 2^{13} = 8kBL$$

Pages

32



$$2^{12} = 4kB$$

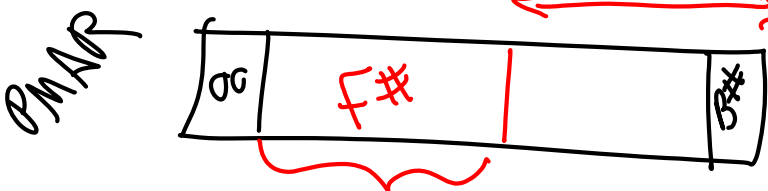
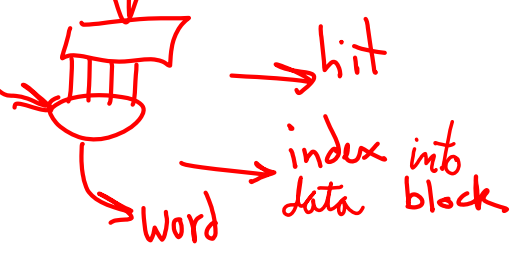


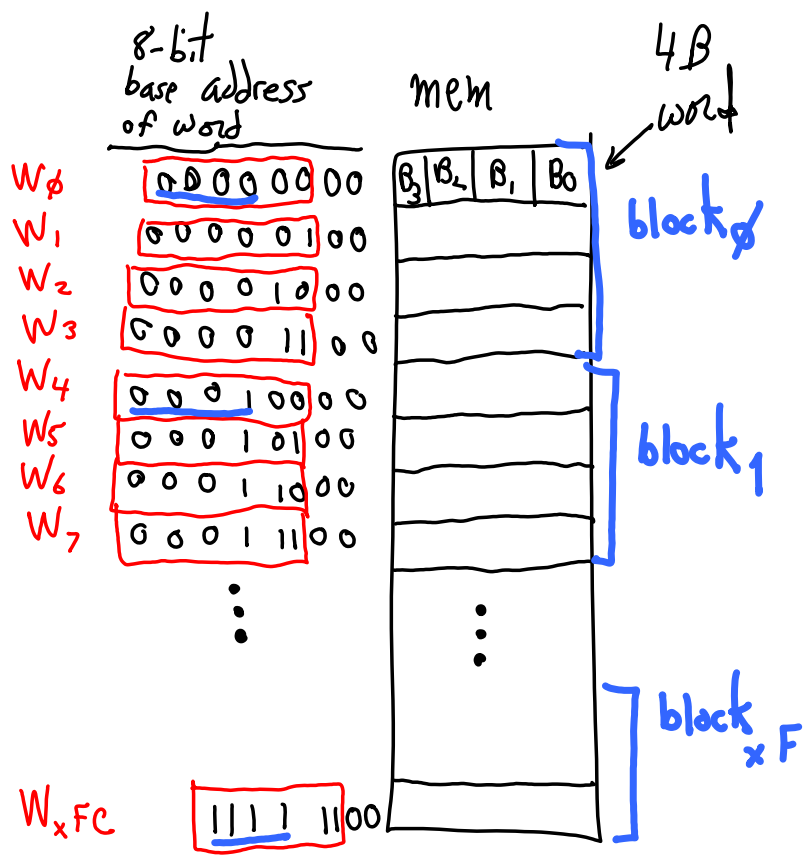
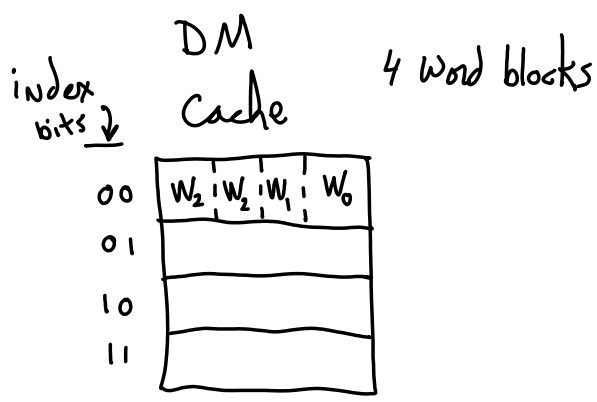
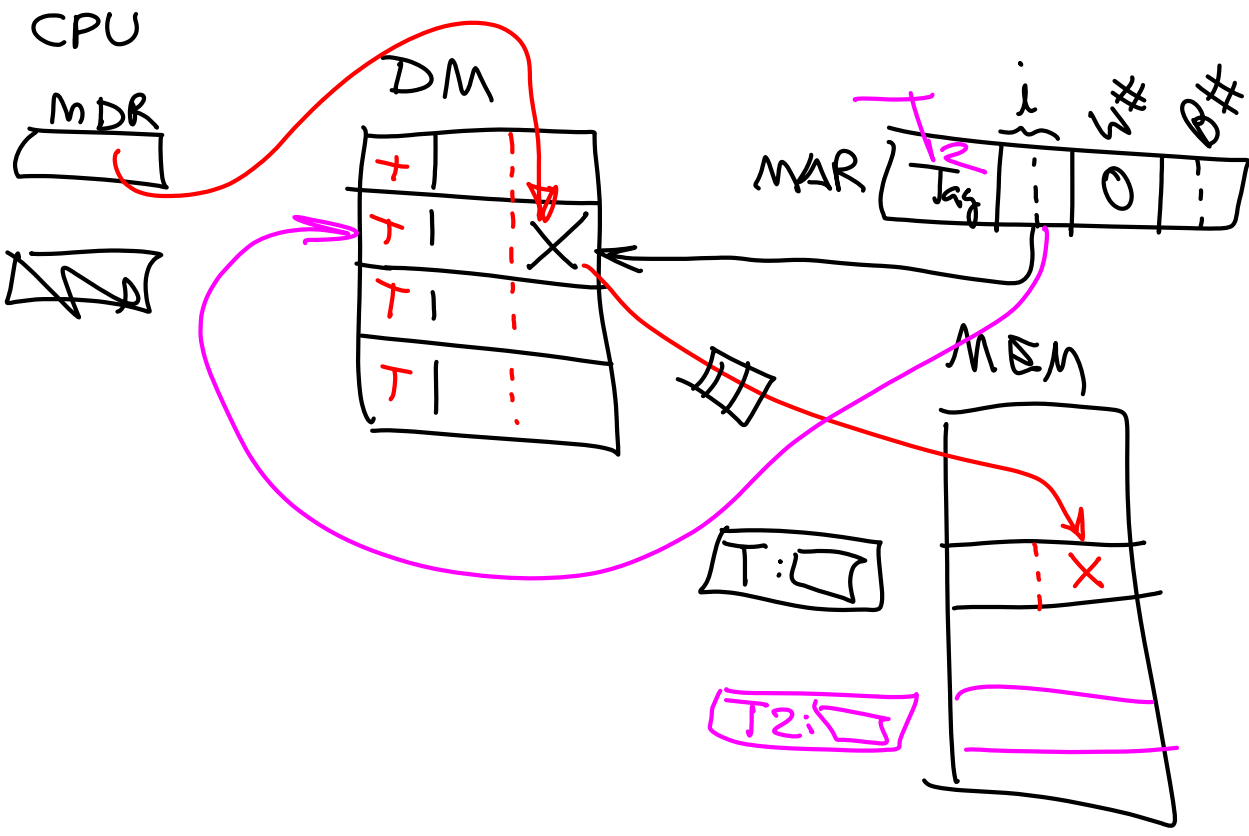
2^{23}
 $8 \cdot 2^{20} = 8M$

$16 \times (32B_{bl} + 23b_{bl})$

size line

- +V
- +D
- +A

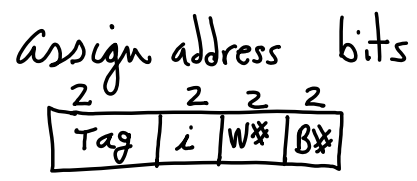


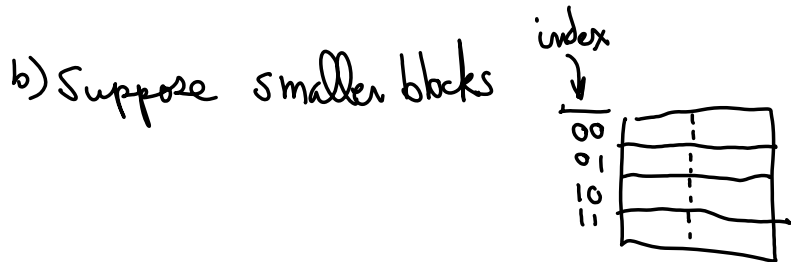
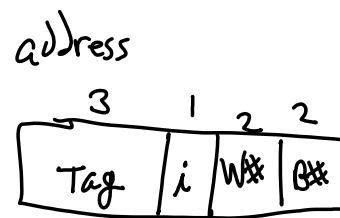


(8-bit address) → 2^8 B Memory
 (byte addressable)

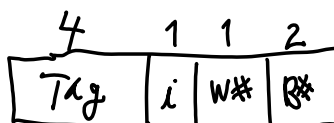
$$2^8 \text{ B mem} \left(\frac{W}{4 \text{ B}} \right) = 2^6 \text{ W mem}$$

$$2^6 \text{ W mem} \left(\frac{\text{block}}{4 \text{ W}} \right) = 2^4 \text{ block memory}$$

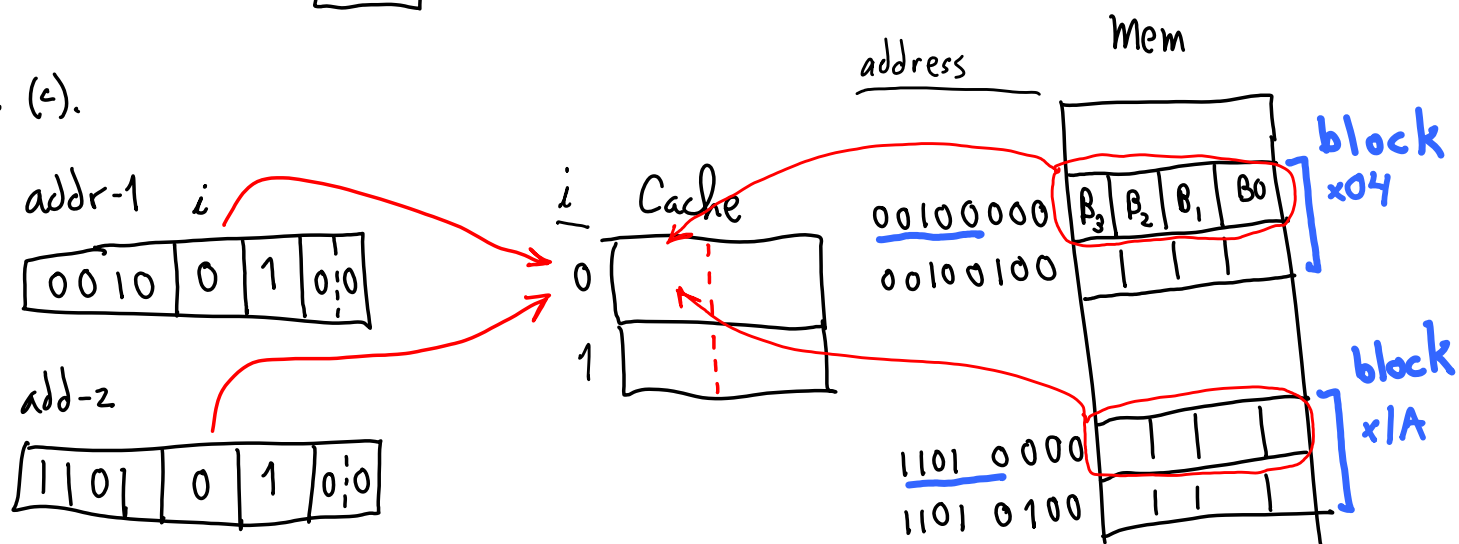




c) Suppose a) and b)



Suppose (c).

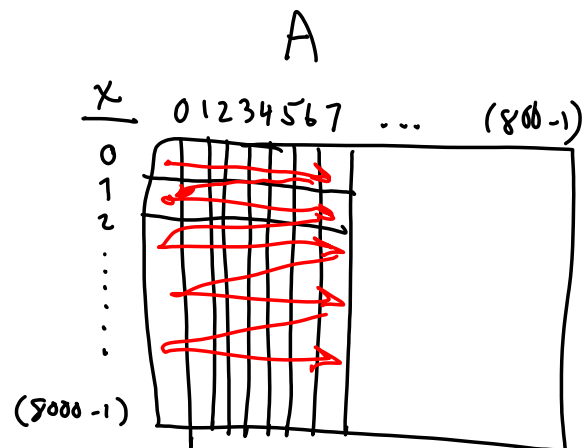
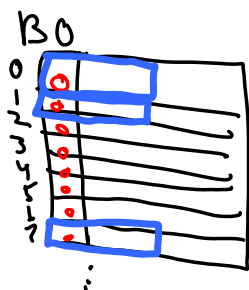


$$x \ 0 \rightarrow (8000-1)$$

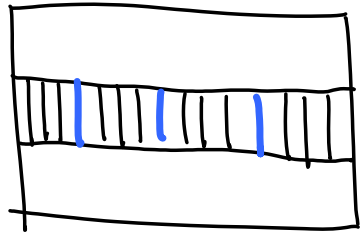
$$y \ 0 \rightarrow 7$$

$$A[x][y] = B[y][0] + A[y][x]$$

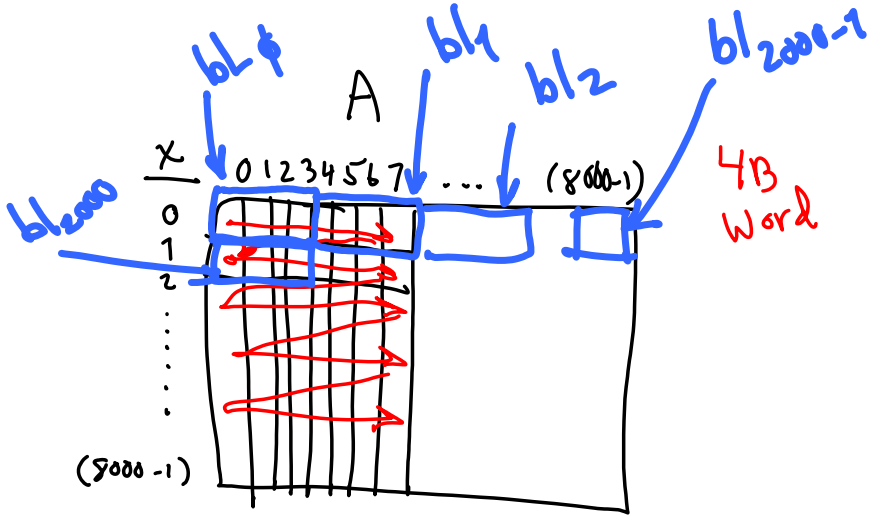
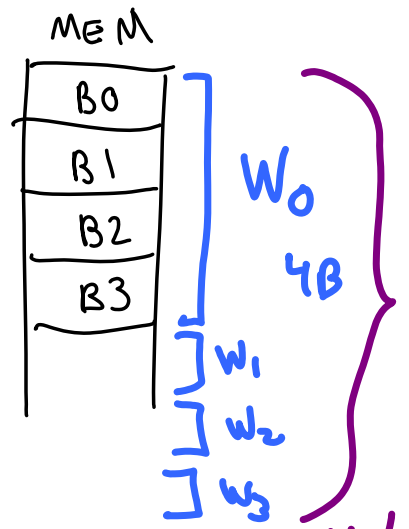
8 blocks



cache

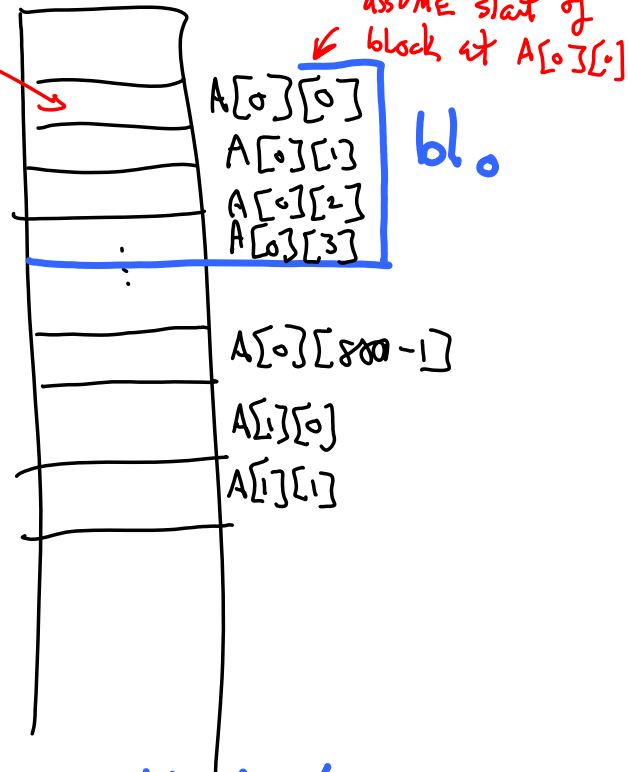


$\leftarrow (16 B) \text{ block}$
 $4 W$

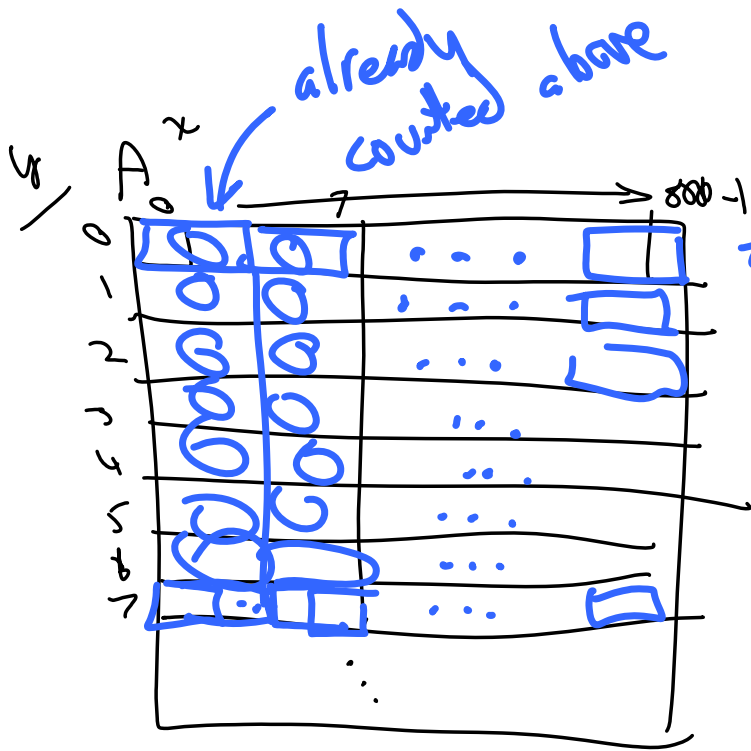


4B Word

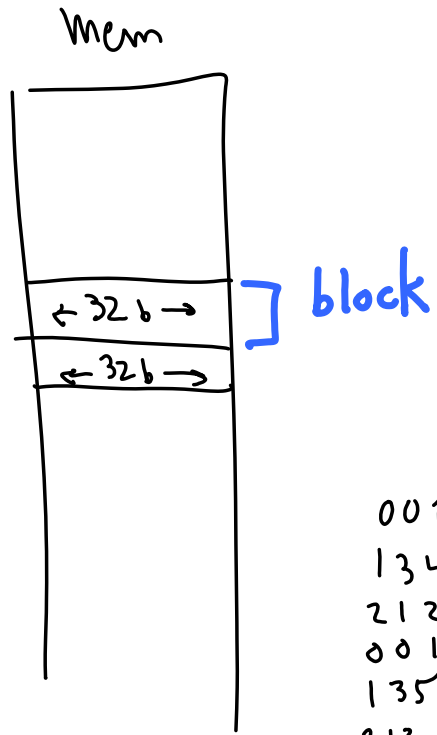
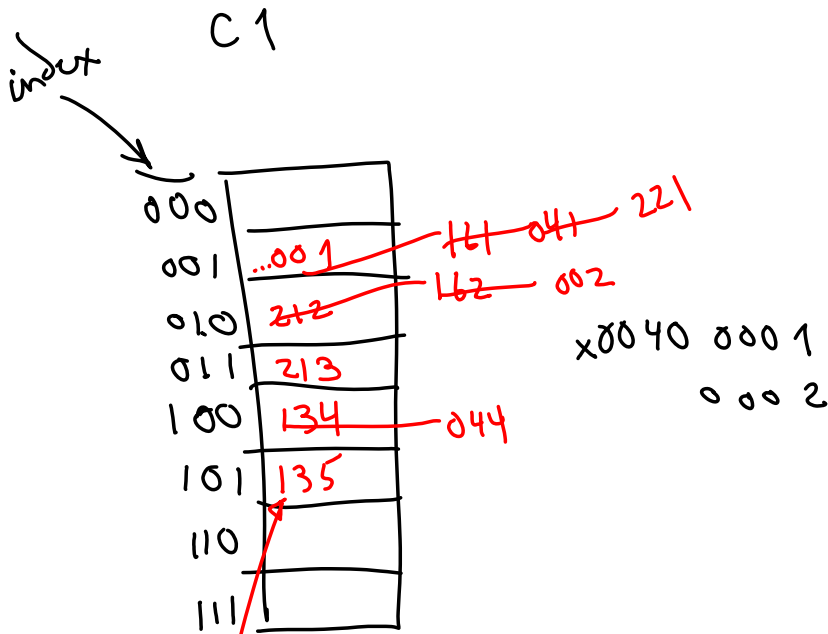
mem



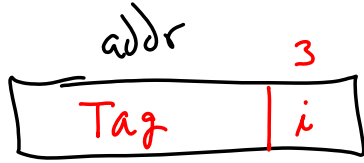
$\left(\frac{2 \text{ blocks}}{\text{row}} \right) 8000 \text{ rows} = 16,000 \text{ blocks}$



2000 blocks/row
 \times
 8 rows
 $= 16,000 \text{ blocks}$
 $- 16 \text{ blocks}$
 (counted twice)

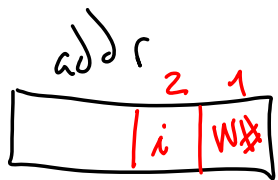


MEM[...135]

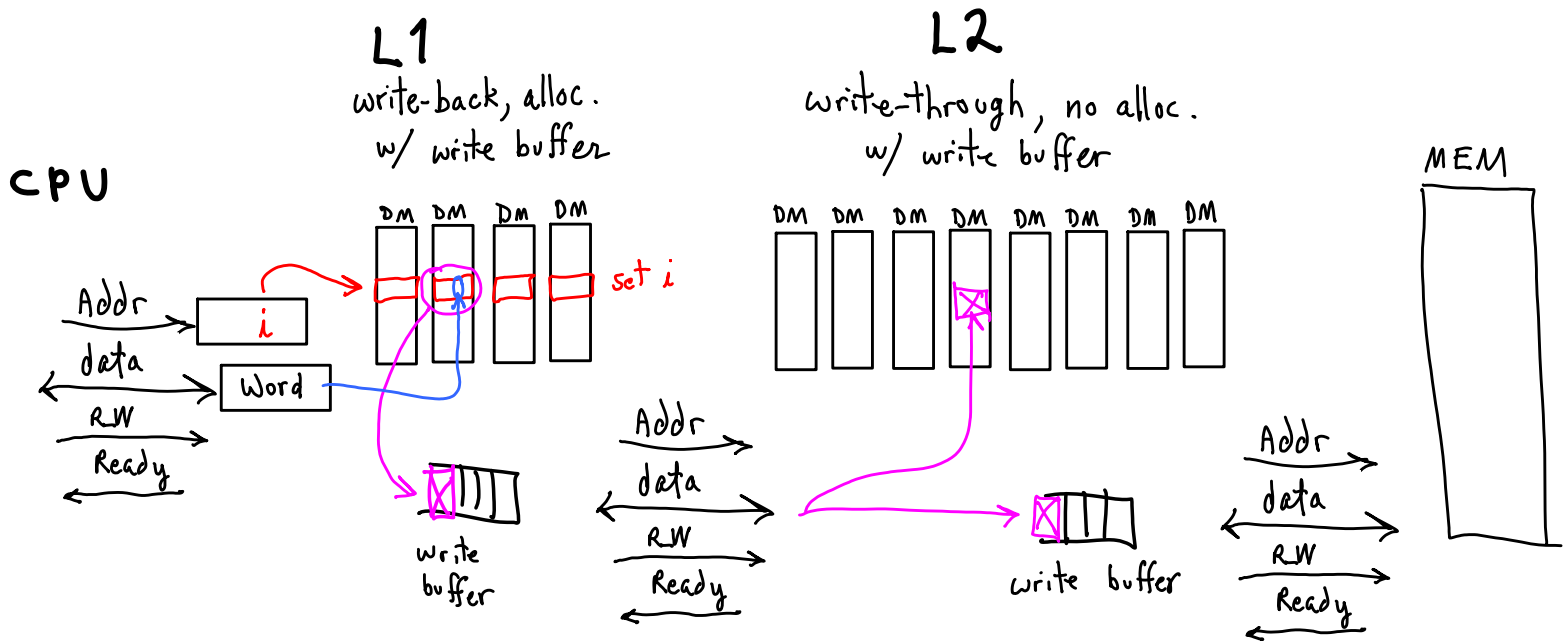


W#? B#?
0 bits 0 bits

- 001 → 0001 M
- 134 → 0100 M
- 212 → 0010 M
- 001 → 0001 H
- 135 → 0101 M
- 213 → 0011 M
- 162 → 0010 M
- 161 → 0001 M
- 002 → 0010 M
- 044 → 0100 M
- 041 → 0001 M
- 221 → 0001 M



- 001 → 0001 M
- 134 → 0100 M
- 212 → 0010 M
- 001 → 0001 H
- 135 → 0101 H
- 213 → 0011 H
- 162 → 0010 M
- 161 → 0001 M
- 002 → 0010 M
- 044 → 0100 M
- 041 → 0001 M
- 221 → 0001 M



L1: (pick victim from set i ☹)

* (write victim if dirty) Send to L2 via buffer $\left\{ \begin{array}{l} [Addr] = [TAG, i, W^* = 0, B^* = 0] = \text{address of victim} \\ [data \text{ block of victim}] \end{array} \right.$

** (Send read request to L2) $\left\{ \begin{array}{l} [Addr] = \text{address from CPU} \\ [R_W = \text{Read}] \end{array} \right.$

(Send L1. Ready to CPU)

(On L2. Ready)

(get data block from L2. data, put it + tag in victim's entry)

(write word from CPU. data to block, set dirty)

* L2: (write victim block to buffer)
(if hit for victim's Addr, write victim block to cache)

** L2: (if hit for Addr, send block to L1)

(else)

(Send [Addr, R/W = Read] to Mem)

(Wait Mem. Ready)

(write block to cache)

(send block to L1)

