MUXes Labeled

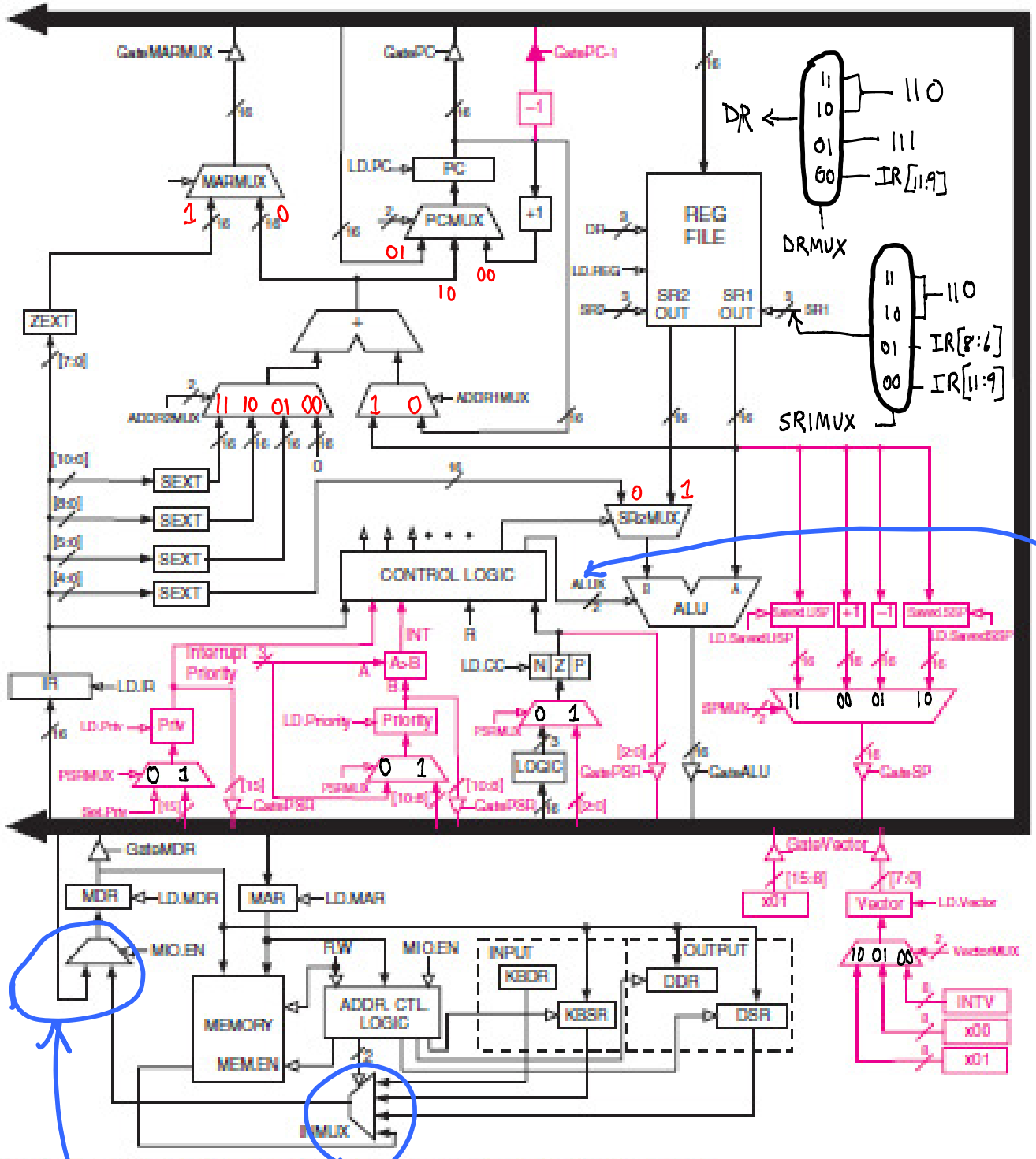
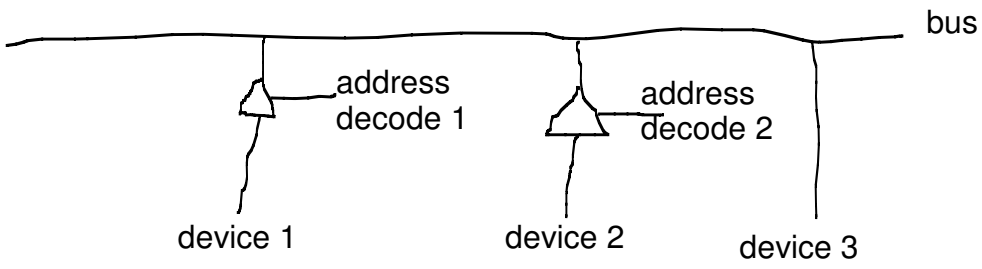


Figure C.3 LC-3 data path, including additional structures for interrupt control

ALUK MUX

00 - ADD
01 - AND
10 - NOT
11 - Pass A

These are layed out in a I/O Bus arrangement (see below)



One of two bus inputs can be selected to feed device 3. The bus is a 2x1 mux. The select signals are control connections to the tri-states: logic receives input and decodes it to enable one of the tri-states. On the memory-IO bus the input to the logic is the memory address on the address bus. Decoder logic is in the individual address logic attached to each device.