PP, Chp 5, problems:

5.4 (#address bits, PC-relative offset size and value)
5.5 (addressing modes and operand locations)
5.7 (largest pos. immed. value)
5.9 (cc+br = nop?)
5.10 (given instr. bits, instr. diff?)
5.11 (immed. data limits)
5.13 (reg-reg transfer, sub, cc set, cc codes, clear reg)
5.14 (OR)
5.18 (#mem accesses LDR, STI, TRAP)
5.21 (#trap routines)

PP, Chp 6, problems:

6.4 (prog. to compare R1 and R2: GT, EQ, LT)

Reading:
PP, Chp. 5: The LC-3 ISA, datapath, and controller.
PP, Chp. 6.2: Using the LC-3 simulator

(NB--PP describe their Simulate.exe, which is very close to what we are using, PennSim.jar. The major difference is that PennSim will not execute an instruction with all zeroes, which is a flaw because such an instruction is a perfectly valid LC3 branch instruction.)