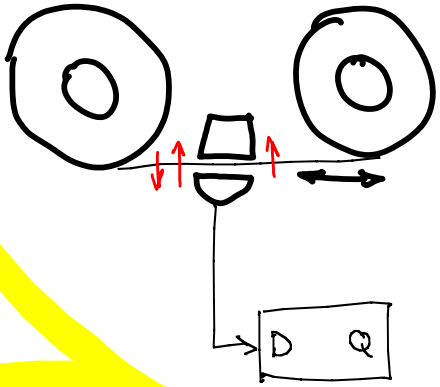
TAPE, kinds of tape

mag/paper tape

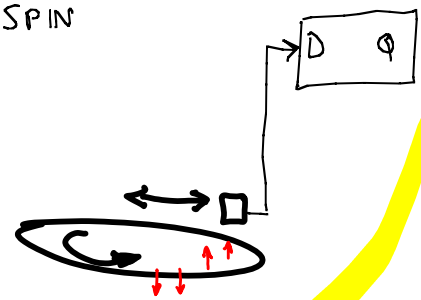


move L/R

R/W Head

mag/optical disk

move IN/out + SPIN



Paper cards

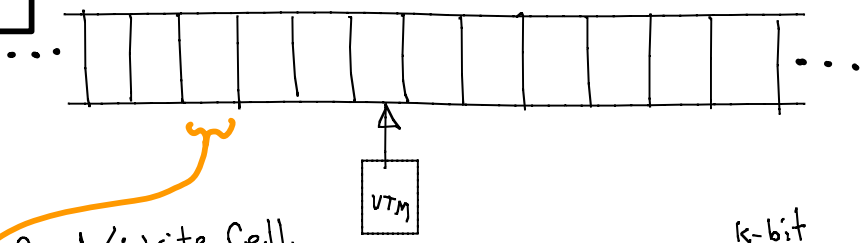
mag/optical/mechanical, move L/R

Communications

one-way tapes

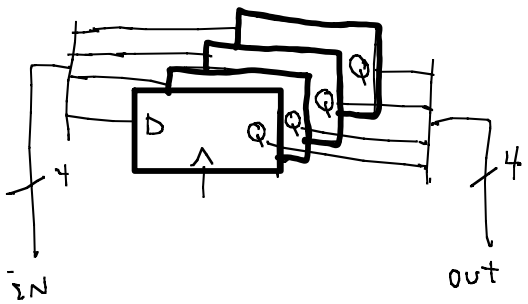
Keyboards, sensors,
monitors, motor controls,
Networks, etc.

TAPE/MEMORY



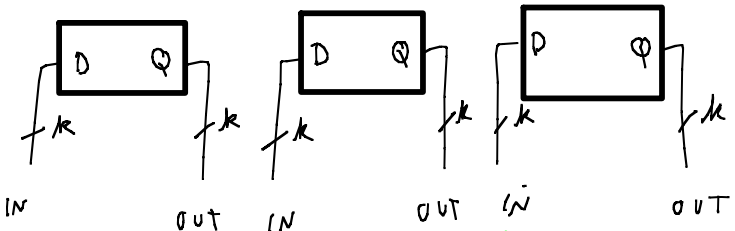
Read/write Cell, k-bit symbol

e.g., 4-bit cell



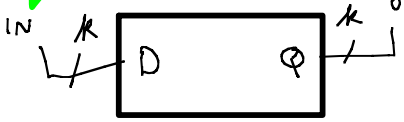
k-bit memory
Register/word/cell

k-bit Cell



Read

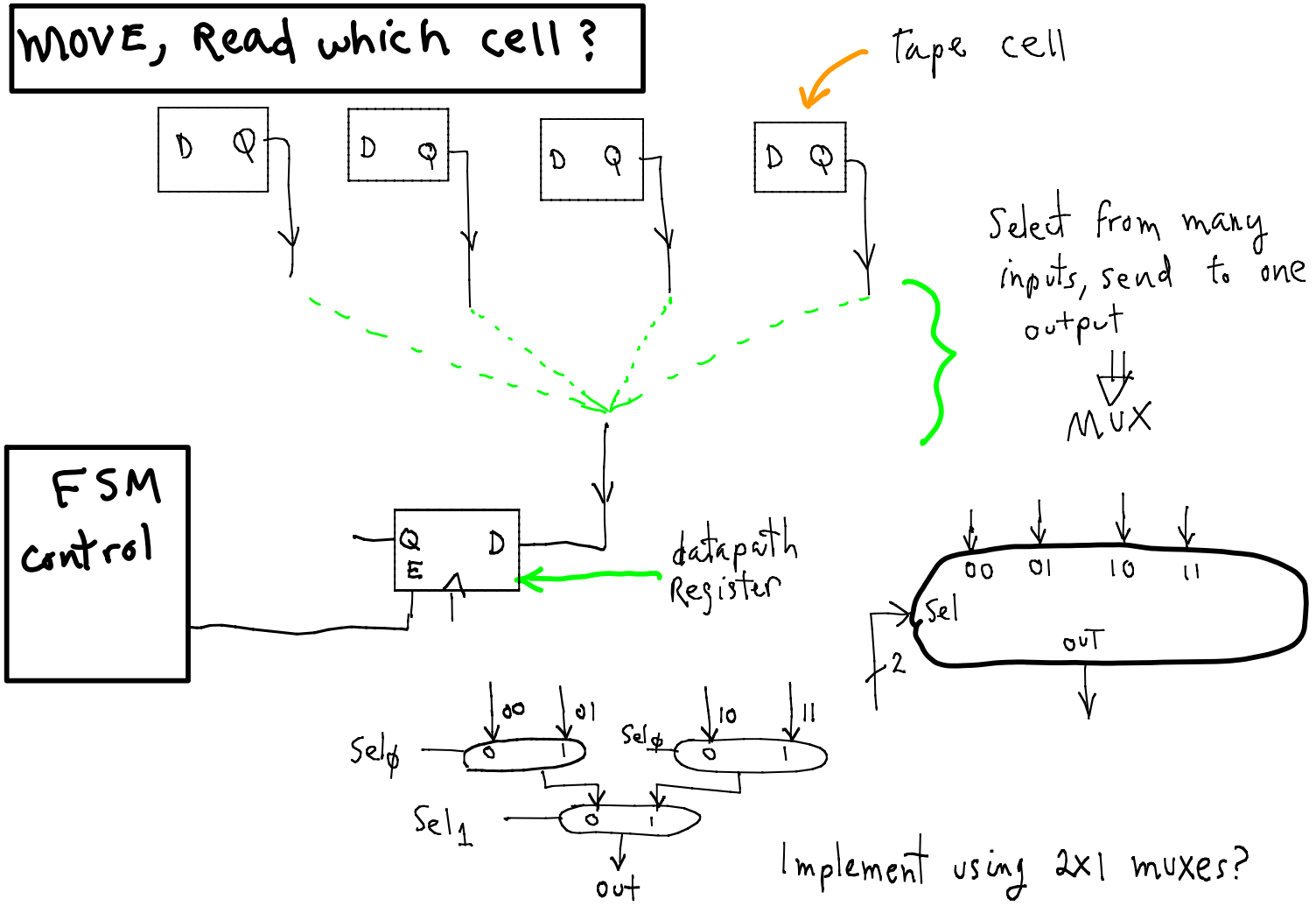
WRITE



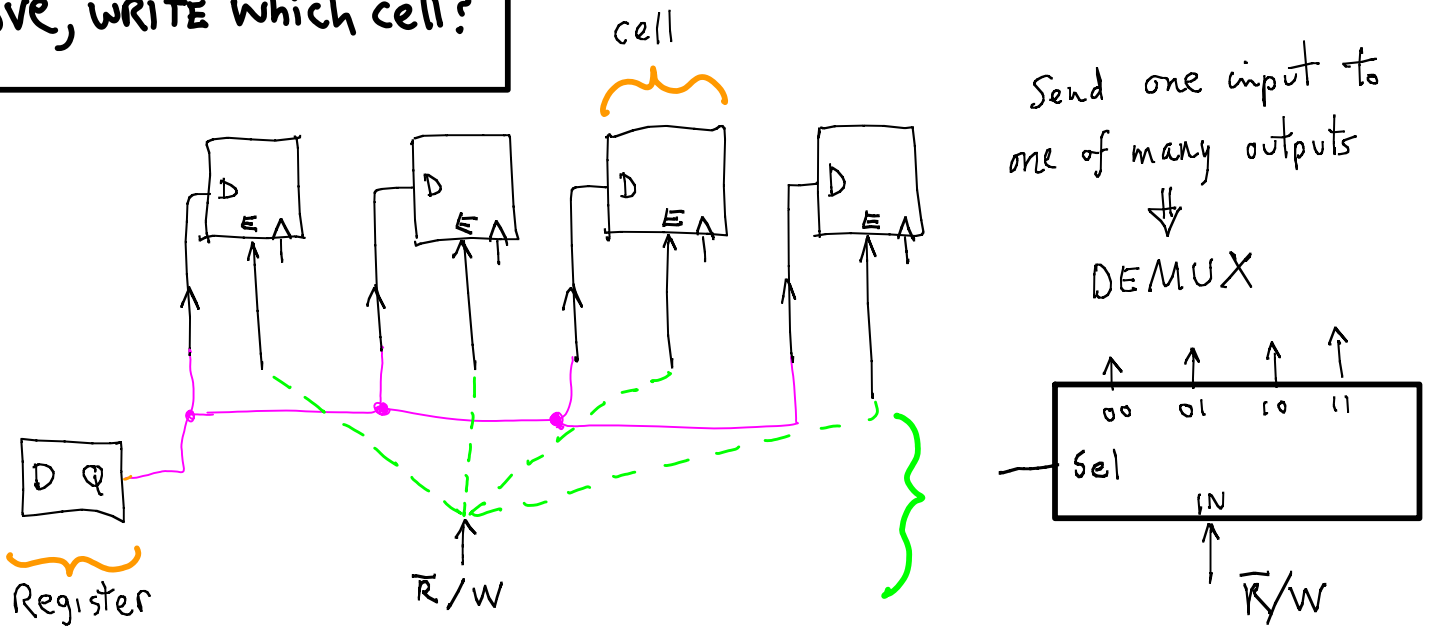
datapath Register

moving L/R?

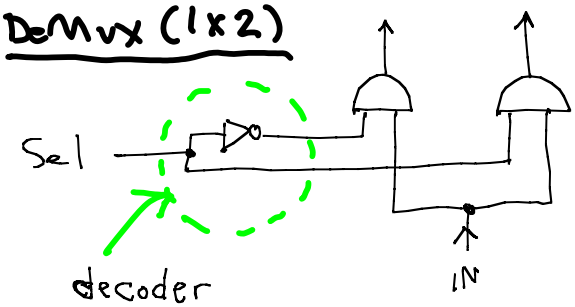
MOVE, Read which cell?



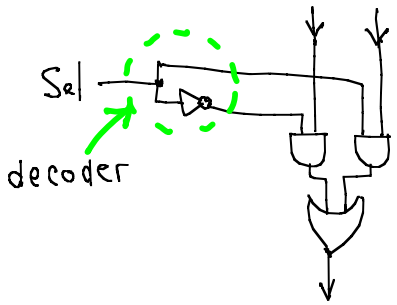
MOVE, WRITE which cell?



DeMux (1x2)

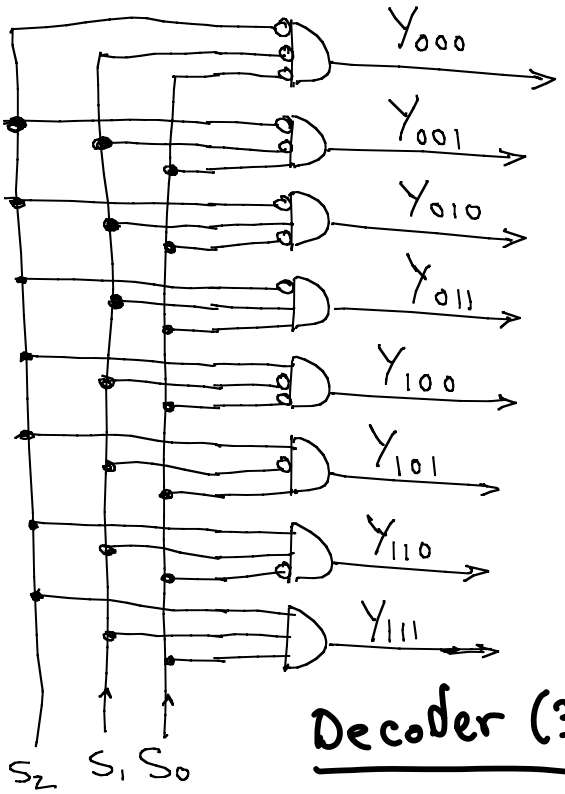


MUX (2x1)



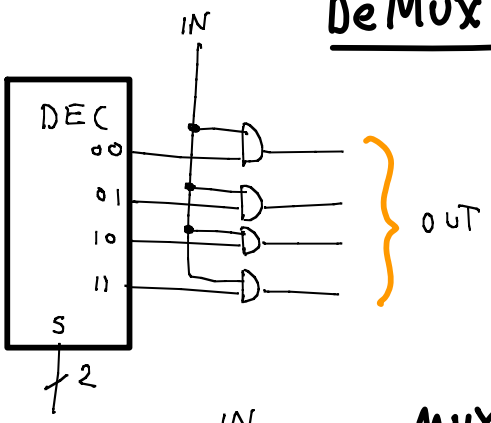
Decoder

exactly one output = 1

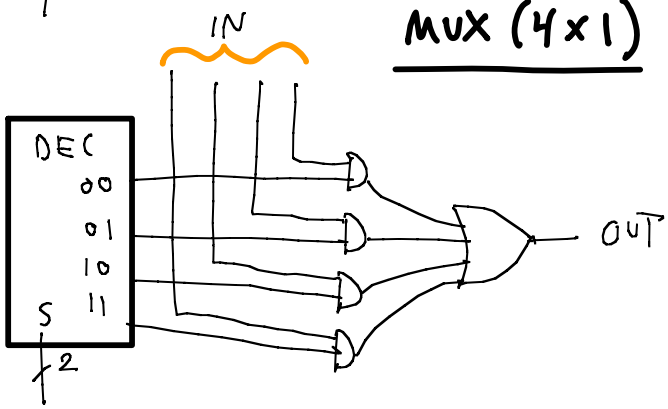


Decoder (3×8)

DeMux (1×4)



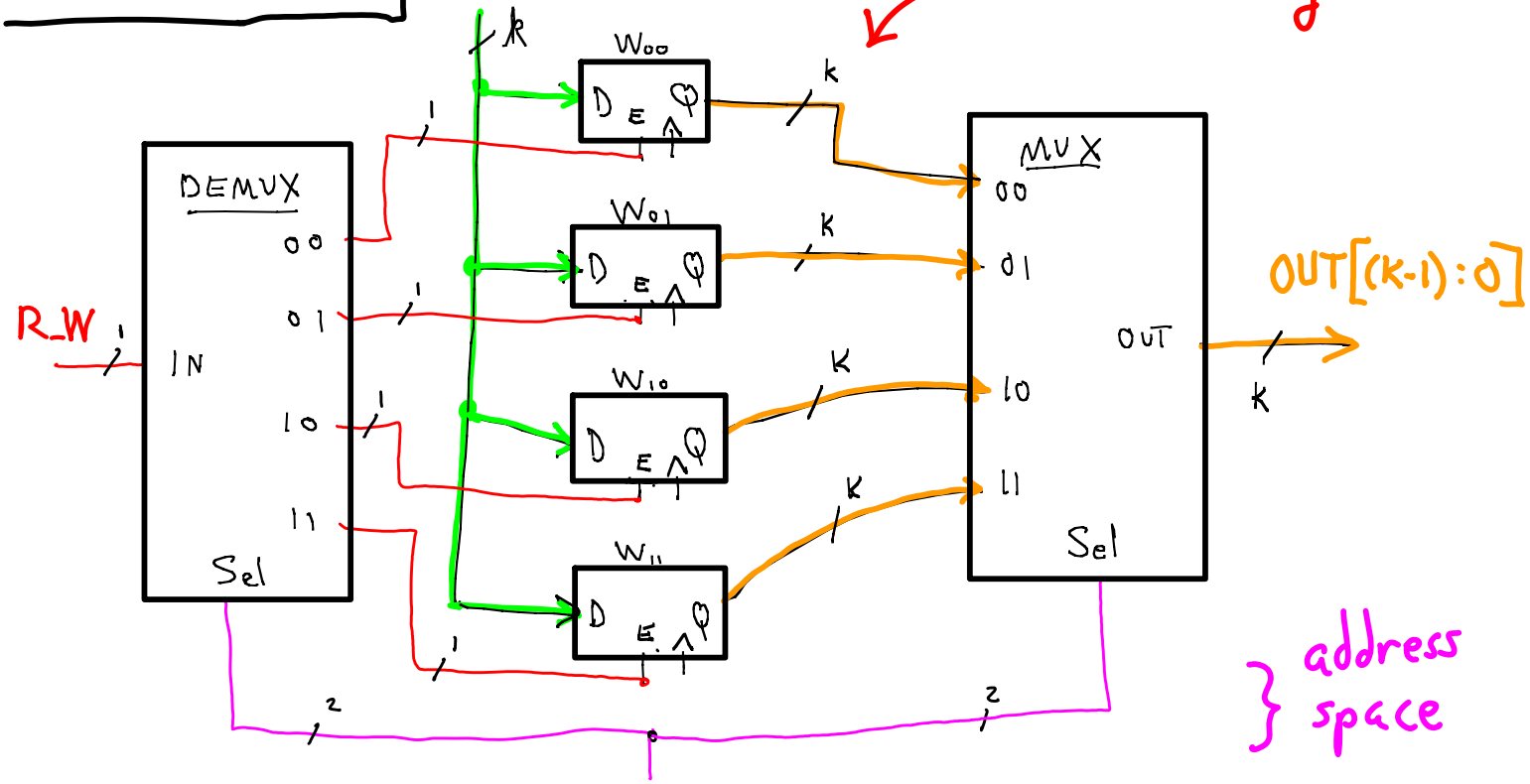
MUX (4×1)



RAM/MEM

IN[(k-1):0]

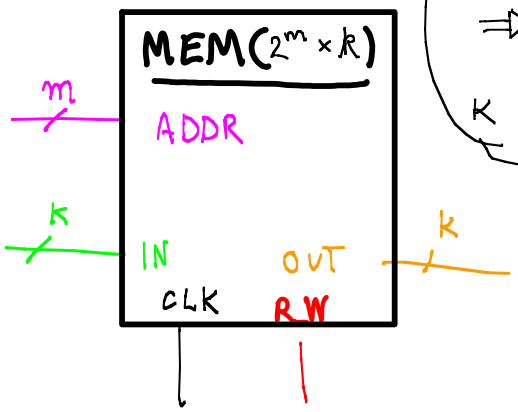
addressability



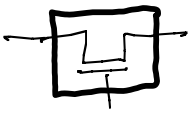
WRITE A Cell

Read a cell

MEM, Rows + Cols

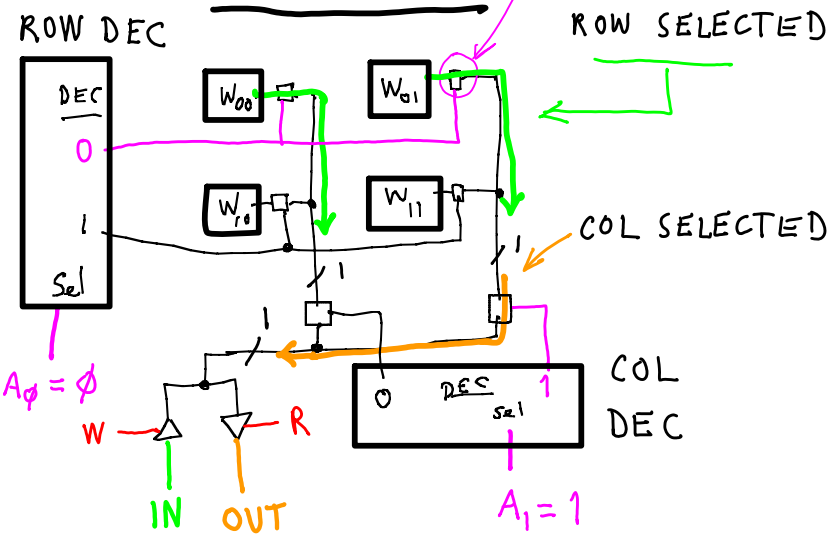


M address bits
$\Rightarrow 2^m$ cells/WORDS
K data bits per word

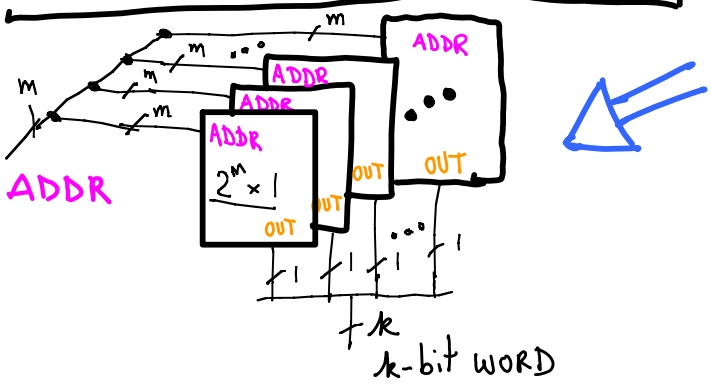


pass/no-pass tr.: allow current or not. Read: cell charges col. line or drains it. Write: cell input gate is charged/drained. Neither R/W: ???

MEM(4 × 1)

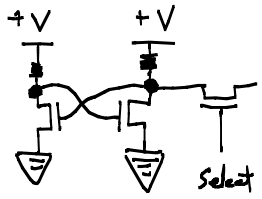


Smaller decoders, fewer logic levels, faster



Cells, SRAM, DRAM | Tri-state

SRAM cell



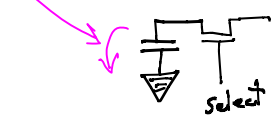
Voltage in forces state change

SRAM: static,
fast, large size per bit ==> small memory

DRAM: dynamic (needs recharge),
slow, small size per bit ==> BIG memory

Charge Leaks away

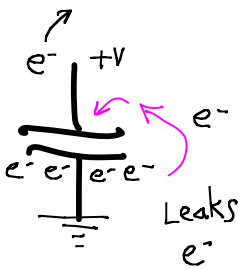
DRAM cell



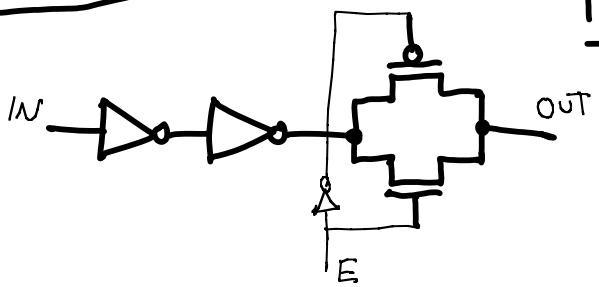
Voltage charges Capacitor

$\Rightarrow$ Read–rewrite refresh cycle needed: slower

Capacitor charged



TRI-STATE Buffer

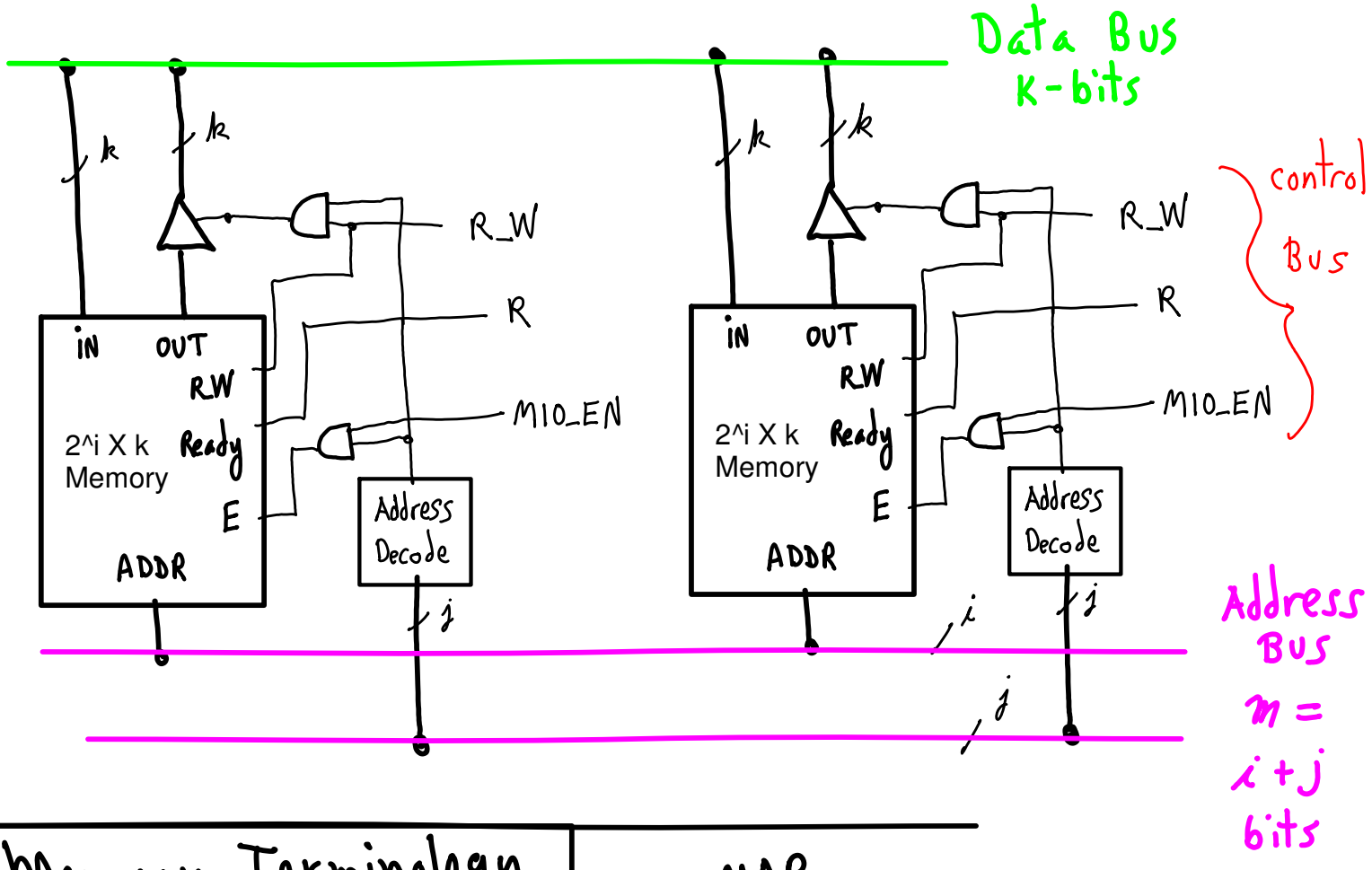


E = 0, no conduction
E = 1, conduction

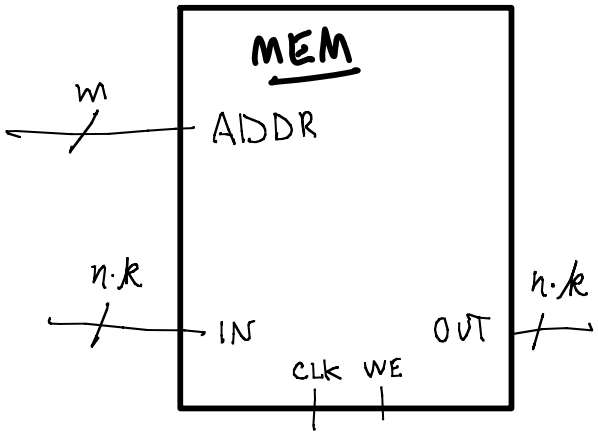
Bus -level organization

2^j memories, each (2^i X k), m = i+j

== One (2^m X k) memory

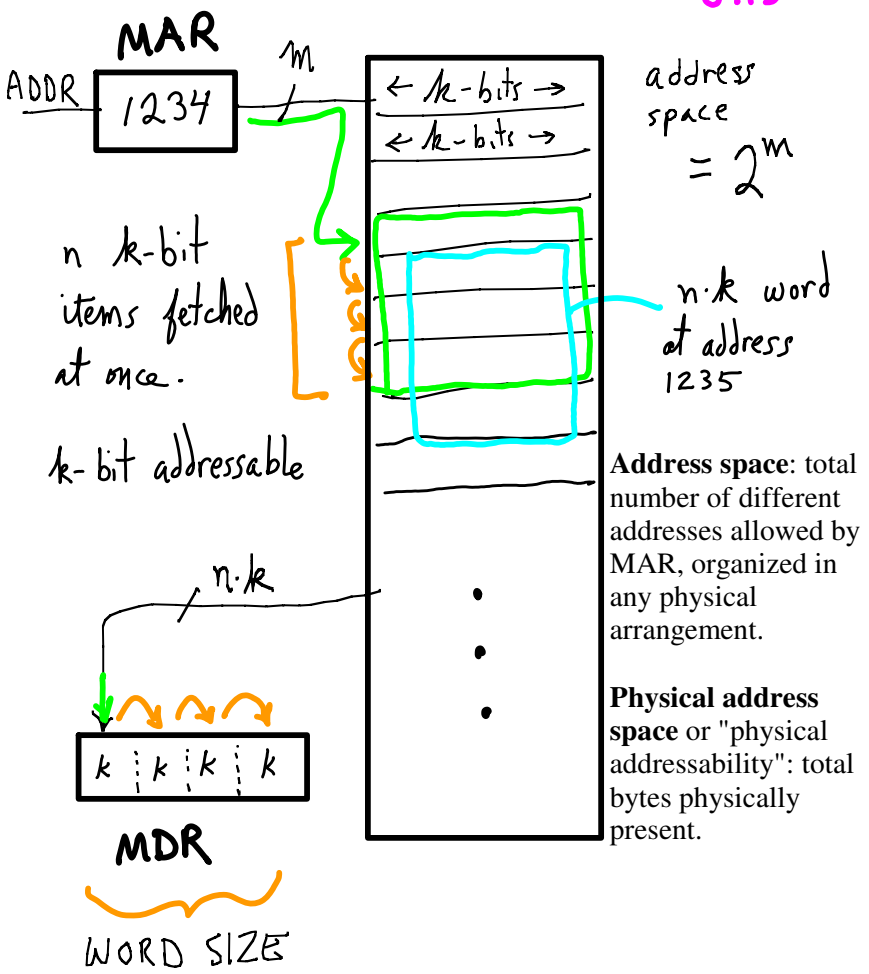


Memory Terminology



k-addressibility: increasing MAR by 1 aligns MDR k bits further in memory. Eg., "byte-addressable" means increasing address by one moves 1 byte forward in memory. NB--"Addressibility" sometimes refers to total memory size or total address space.

word size: number of bits in MDR. Often, same as number of bits ALU processes as a word. But, MDR might contain multiple ALU words: then it is called the memory **line size**.

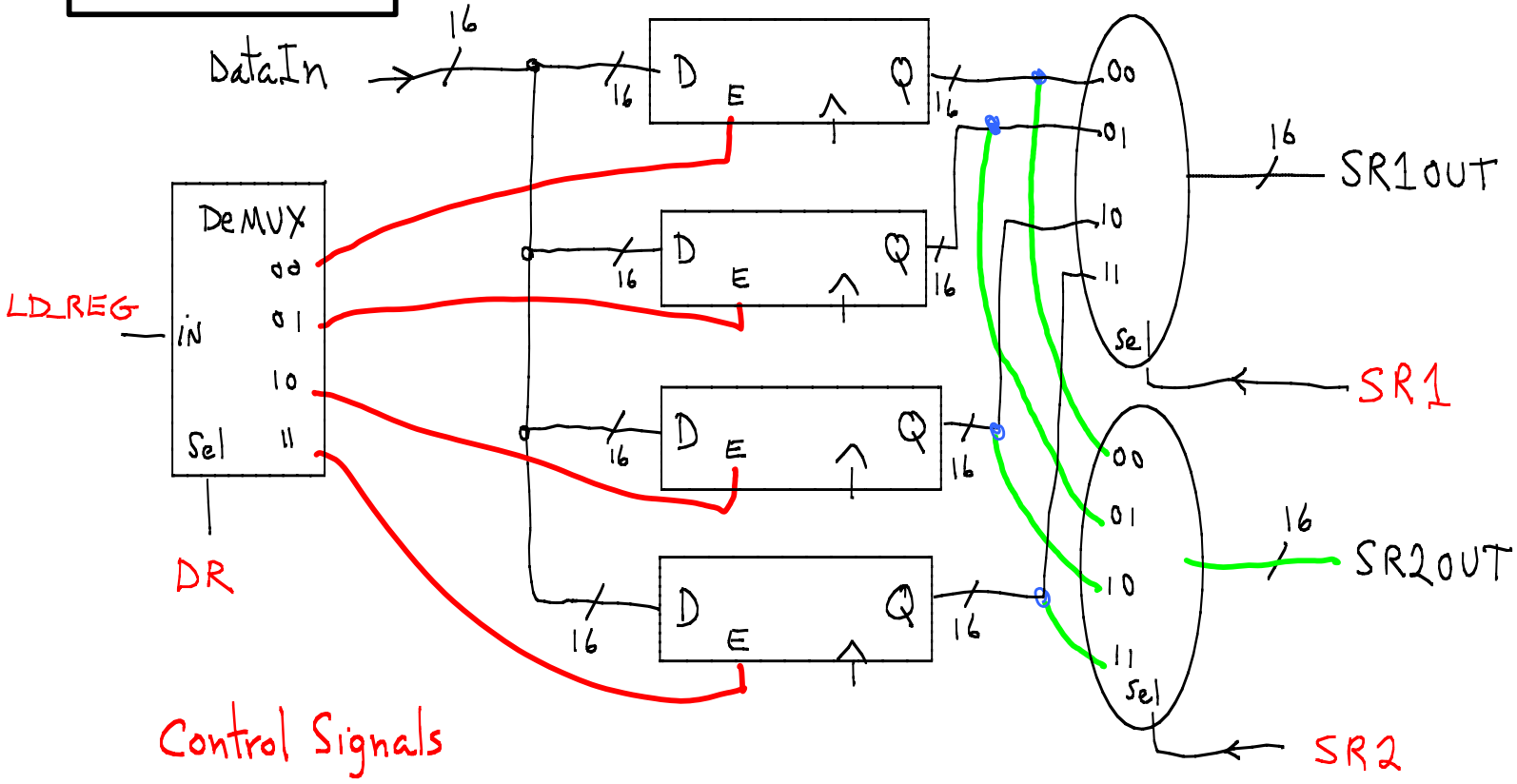


Address space: total number of different addresses allowed by MAR, organized in any physical arrangement.

Physical address space or "physical addressability": total bytes physically present.

Reg file

A little (fast) memory, with multiple read and/or write ports.



Next

We have: FSM controller
functions, registers for datapath
Tape (RAM, etc.)

Need: encoding for descriptions (LC3 ISA)
encoding for data
functional units for operations on data (ALU)