Reading: PP-chp 3:

3.3 (decoder, mux, FA, PLA)
3.4 (R-S latch, register)
3.5 (memory)
3.6 (sequential machines, FSM)
3.7 (LC-3 datapath)

§ Problems, PP-chp 3:
§ 3.12 3-Dec, show minterm exp.
§ 3.13 5-dec, show num output lines.
§ 3.14 16X1 mux, how many select lines?
§ 3.19 explain mux ckt, s-r latch
§ 3.20 truth table => trans. Ckt -(-a.b)
§ 3.22 4X1 mux, from 2x1 MUXs
§ 3.24a 2x1 mux, identify input (select)
§ 3.29 d-latch transparency
§ 3.30a 2-in-3-out comparator truth table.
§ 3.30c, 4-bit EQUAL from 1-bit 2X3 comparators
§ 3.31 #word X word_size = mem. Size
§ 3.32, addressability vs. address
§ 3.33a row X col addressing: find 4-th word
§ 3.33b #selects for 60 words?
§ 3.33c #words max for #select=3?
§ 3.43a fsm truth table
§ 3.43b state diagram for (a)