

Lec-6-HW-4-VLSIpower

VLSI

We talked about the nature of device fabrication in silicon. Signal current flows through the gate channel. While the voltage drop across wires is negligible, this channel current flows across a voltage drop. (We did not discuss in class how much voltage drop there is across the transistor channel. We can simply assume it is some fixed V .) Note that in CMOS design, current only flows (except for leakage currents) during transistor switching: the p-transistor charges the output wire up to V_{cc} when the output changes from 0 to 1; the n-transistor drains it down to ground whenever the output changes from 1 to 0. We'll assume this occurs once per clock tick, and the clock ticks at F cycles per second.

(a.) Explain what this means in terms of power per transistor. That is, assume the channel has resistance R , and a voltage drop of V . Use Ohm's Law, $i = V/R$, and the fact that current (e-/sec) times voltage (energy/e-) is power (energy/sec). NB--You don't have i , use V/R .

(b) The clock ticks F times per second. At each tick, current only flows for a short time, just long enough to charge up the output. Let's say current flows for $1/2$ of each clock cycle; so, overall, one could say that only $i/2$ current actually flows on average since for half the time i current flows, and for the rest of the cycle no current flows. Adjust your answer to (a) to reflect this fact. NB--The current flow rate is the same no matter what F is.

(c.) Given your result for (b), show what this means for power per chip area. Use $A = W \cdot L$ for channel area (W and L are channel width and length), and assume each transistor's total area is proportional to its channel area: ie., total area per transistor = $8 \cdot A$.

(d.) Now, suppose the next generation of chip technology becomes available, and we use the same circuit, but now the new channel dimensions are half size: $W' = W/2$ and $L' = L/2$. This will allow the chip's operating voltage to halve to $V/2$, and clock speed to double to $2 \cdot F$. Assume the channel resistance is proportional to channel length L and thus the new channel resistance is halved as well: $R' = R/2$. What effect does this have on power/area for the new chip?

(e.) What is the effect after k generations of new chips, each changing as in (c)? Noting that this power is heat, what can you say about the prospects for future improvements in chip size and speed.

[NB--The above device parameters are not based strictly on silicon device characteristics. The relationships show an approximate equivalent result where several scaling effects are lumped together to form these pseudo V , R , i , and A parameters and their relationships. Actual device parameters and their relationships affecting power density are more complex.]

